What is claimed is:

1. A method for manufacturing a gate spacer for self-aligned contacts comprising:

forming a gate stack on a semiconductor substrate;

forming a conformal dielectric layer over the gate stack;

applying an etch-stop material layer over the conformal dielectric layer;

removing an upper portion of the etch-stop material layer to expose an upper portion of the conformal dielectric layer;

etching back the exposed conformal dielectric layer;

removing the remaining etch-stop material layer; and

etching back the etched-back conformal dielectric layer to form a gate spacer.

2. The method of claim 1, wherein the gate stack comprises a gate dielectric, a gate electrode, a hard mask, and a patterned oxide layer.

3. The method of claim 2, wherein a top surface of the gate spacer is substantially lower than that of the hard mask.

4. The method of claim 1, wherein a top portion of the gate spacer is approximately 400 Å higher than that of the gate electrode.

5. The method of claim 1, wherein the etch-stop material layer comprises an organic material.

6. The method of claim 5, wherein the etch-stop material layer is a photoresist layer.

7. The method of claim 6, wherein removing the photoresist layer comprises etching the photoresist layer using a gas mixture of SF_6, CF_4, O_2 and HBr.

8. The method of claim 1, wherein the etch-stop material layer is used as an etch stopper during etching of the exposed conformal dielectric layer.

9. The method of claim 1, wherein a thickness of the etch-stop material layer is more than approximately 1000 Å.

10. A method for manufacturing a semiconductor device comprising:
forming a gate stack on a semiconductor substrate;
forming a gate spacer on sidewalls of the gate stack, wherein the gate spacer includes a top portion substantially lower than a top of the gate stack.

11. The method of claim 10, further comprising forming an interlayer insulating layer over the gate stack including the gate spacer.

12. The method of claim 11, before forming an interlayer insulating layer, further comprising forming a blanket etching stop layer over the gate stack and the semiconductor substrate.

13. The method of claim 11, further comprising forming a self-aligned contact hole within the interlayer insulating layer adjacent the gate stack.

14. A method of claim 13, further comprising:
depositing a conductive material within the contact hole; and
planarizing the conductive material to form a contact pad.